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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,364	03/23/2004	Han-Chung Lai	250122-1440	3950
24504	7590	09/20/2005	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			PARKER, KENNETH	
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary**Application No.**

10/807,364

Applicant(s)

LAI, HAN-CHUNG

Examiner

Kenneth A. Parker

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-5 and 7-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Ukita 6310668.

Ukita shows several embodiments (mainly indicated as prior art) relevant to the current claims having compensation structures including figure 11 and 14 which have two downward portions of gate 33; and figure 16 which has a wrapped bottom portion of gate 33. Regarding claim 1, the Ukita reference shows a liquid crystal display device with a capacitance-compensated structure, comprising: a gate line 33; a gate electrically connected to the gate line 32; a compensation structure connected to the gate figure 11 element 61; figure 14 element 34; figure 16, the wrapped bottom portion of 32; and a drain having a first side opposite to a second side (pixel electrode 42), wherein the first side of the drain overlaps the gate (region 40) and the second side of the drain overlaps the compensation structure (region 62). Please note that the language “connected to” as must include “indirectly connected to”, as dependent claim 2 has the structure extending from the gate line, implying that a structure that extends from the gate line meets the constraint of being connected to the gate.

The reference shows regarding claim 2 wherein the compensation structure extends from the gate line (element 61 does).

The reference shows regarding claim 3 wherein the compensation structure extends from the gate- the right portion 40 doesn't act as a gate, therefore it can be construed as part of the compensation portion, and "extending" from the gate as it extends to the right and or left of the portion where it acts as a gate.

The reference shows regarding claim 4 wherein the compensation structure comprises two portions, in which one extends from the gate line and the other extends from the gate (see descriptions of 3 and 4 above).

Regarding claim 5, the Ukita reference shows a liquid crystal display device with a capacitance-compensated structure, having a gate line and a data line to turn a thin film transistor on or off, comprising: a gate 32 electrically connected to the gate line 33; a drain 42 having a first side opposite to a second side, wherein a first parasitic capacitor is formed between the first side of the drain and the gate and a second parasitic capacitor is formed between the second side of the drain and the gate (overlaps always create parasitic capacitors, so this limitation is inherent).

The reference shows regarding claim 7 wherein the second parasitic capacitor comprises the second side of the drain and a compensation structure electrically connected to the gate.

The reference shows regarding claim 8 wherein the compensation structure extends from the gate line (61 does)

The reference shows regarding claim 9 wherein the compensation structure extends from the gate - the right portion 40 doesn't act as a gate, therefore it can be construed as part of the compensation portion.

The reference shows regarding claim 10 wherein the compensation structure comprises two portions, wherein one portion extends from the gate line and the other portion extends from the gate (See discussions of claims 9 and 10 above).

Regarding claim 11, the Ukita reference shows a liquid crystal display device with a capacitance-compensated structure, comprising (viewing figure 14):

a first process layer comprising a gate line 33, a gate 32, and a compensation structure 34, wherein the gate is electrically connected to the gate line and the compensation structure connects to the gate; and a second process layer comprising a data line 38, a source (portions of 38 near 39), and a drain 40-41, wherein the source and the drain are formed corresponding to both sides of the gate (as shown),

Art Unit: 2871

respectively, the source is electrically connected to the data line (as shown), the data line is substantially perpendicular to the gate line (portions are and the overall line runs perpendicular, so is viewed as meeting "substantially perpendicular), further, the vertical portions can be considered the data line), the drain has a first side overlapping the gate (hence the dotted lines 39) and a second side overlapping the compensation structure (the shaded area), wherein the first side is opposite to the second side. The limitation that there is an acceptable alignment shift range between the first process layer and the second process layer where between the first side of the drain and the gate and a second parasitic capacitor between the second side of the drain and the compensation structure maintain a substantially constant value within the acceptable alignment shift range the sum of the capacitance of a first parasitic capacitor is met as within a certain shift there will be a compensation in the same manner as with the instant invention.

The reference shows regarding claim 12 wherein the compensation structure extends from the gate line (61 does).

The reference shows regarding claim 13 wherein the compensation structure extends from the gate.

The reference shows regarding claim 14 wherein the compensation structure comprises two portions, wherein one portion extends from the gate line and the other

Art Unit: 2871

portion extends from the gate - the right portion 40 doesn't act as a gate, therefore it can be construed as part of the compensation portion.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Ukita 6310668 in view of Fujikawa 5995178.

The reference lacks regarding claim 6 wherein a capacitor dielectric layer of the first parasitic capacitor comprises two portions wherein one portion is a stacked structure comprising a gate insulating layer, a semiconductor layer and a channel protection layer, but shows and the other portion is a stacked structure comprising the gate insulating layer and the semiconductor layer, a capacitor dielectric layer of the second parasitic capacitor is a stacked structure comprising the gate insulating layer and the semiconductor layer, simply because a TFT has to have the gate insulator and the semiconductor layer. So what is actually lacking is the presence of a channel protection layer, which would give the two different regions of the first parasitic capacitor. Fujikawa teaches the use of a channel protection layer for the benefit of having it act as an etch stop layer (bottom column 1), but it was also well known for

protection of the back of the channel from effects such as contaminants (hence the name back channel protection layer). Therefore one of ordinary skill would have found reason, suggestion or motivation to employ a back channel protection layer for the benefits mentioned above. Please note that in Fujikawa figure 19, the back channel protection layer only partly fills the space between the drain and the gate, and therefore creates two regions, one with a back channel and one without. Further please note that the application of this to figure 11 only modifies the TFT portion, so no back channel layer is present under 61, and also regarding figures 14 and 16, the comprising language does not exclude the possibility of the back channel layer being there, it only removes the requirement that it be there.

Conclusion

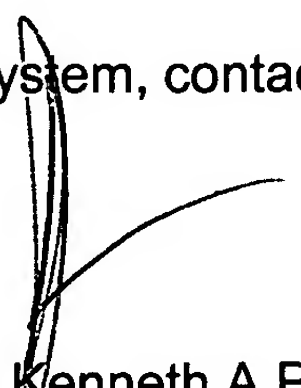
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Muto 4902638; figures 7- 8, the two portions of gate 12

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth A. Parker whose telephone number is 571-272-2298. The examiner can normally be reached on M-F 10:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Kenneth A Parker
Primary Examiner
Art Unit 2871